CLAIMS

What is claimed is:

1. An integrated circuit package structure, comprising:

a substrate having a second surface and a first surface for mounting an integrated circuit chip, wherein the integrated circuit chip has a first region and a second region, and the integrated circuit chip generates more heat in the first region than in the second region;

a plurality of ball pins disposed on the second surface of the substrate; and

a power ring disposed on the first surface of the substrate and around the integrated circuit chip, wherein the power ring is electrically connected to the integrated circuit chip via a plurality of power wires, and the power ring has a larger surface area adjacent to the first region while the power ring has a smaller surface area adjacent to the second region.

2. The integrated circuit package structure of claim 1, wherein the power ring is further electrically connected to the ball pins via a plurality of metal plugs through the substrate.

3. The integrated circuit package structure of claim 1, wherein the power ring is consisted of a plurality of blocks without linking to each other, and the surface area of parts of the blocks neighboring the first region is larger than the surface area of other parts of the blocks neighboring the second region.

4. The integrated circuit package structure of claim 1, wherein the integrated circuit chip is a core logic chip.

5. The integrated circuit package structure of claim 1, wherein a heat-dissipating metal upper cap covers top of the substrate and the integrated circuit chip.

6. The integrated circuit package structure of claim 5, wherein the heat-dissipating metal upper cap is composed of aluminum metal.

7. The integrated circuit package structure of claim 1, wherein the substrate is electrically connected to a multi-layer circuit board via the ball pins.

8. The integrated circuit package structure of claim 7, wherein the multi-layer circuit board comprises an isoelectric conducting layer and a plurality of through holes, and the ball pins electrically connects to the isoelectric conducting layer of the multi-layer circuit board through the through holes, and the heat generated by the integrated circuit chip is dissipated via said isoelectric conducting layer.

9. The integrated circuit package structure of claim 8, wherein the isoelectric conducting layer is a power layer or a ground layer.

10. The integrated circuit package structure of claim 7, wherein the multi-layer circuit board is a computer motherboard.

11. An integrated circuit package structure, comprising:

a substrate having a first surface provided for mounting an integrated circuit chip;

a plurality of pins disposed on a second surface of the substrate;

a power ring disposed on the first surface of the substrate and around the integrated circuit chip, wherein the power ring is electrically connected to the integrated circuit chip, and the power ring is further electrically connected to the substrate for heat dissipating; and

a heat-dissipating metal upper cap disposed on top of the integrated circuit chip, having a first cap surface facing the integrated circuit chip, forming a space between the heat-dissipating metal upper cap and the integrated circuit chip, and

having a second cap surface for dissipating heat contacting external air.

12. The integrated circuit package structure of claim 11 wherein the integrated circuit chip has a first region and a second region, the integrated circuit chip generates more heat in the first region than in the second region, the power ring is consisted of a plurality of blocks without linking to each other, and the surface area of parts of the blocks neighboring the first region is larger than the surface area of other arts of the blocks neighboring the second region.

13. The integrated circuit package structure of claim 11, further comprising a plurality of ball pins disposed on a second surface of the substrate.

14. The integrated circuit package structure of claim 11, wherein the power ring is electrically connected to the chip via a plurality of power wires, the power ring is further electrically connected to the ball pins via a plurality of metal plugs through the substrate.

15. The integrated circuit package structure of claim 11, wherein the heat-dissipating metal upper cap is composed of aluminum metal.

16. The integrated circuit package structure of claim 11, wherein the integrated circuit chip is a core logic chip.

17. The integrated circuit package structure of claim 11, wherein the integrated circuit chip has a first region and a second region, the integrated circuit chip generates more heat in the first region than in the second region, and the power ring has a larger surface area adjacent to the first region while the power ring has a smaller surface area adjacent to the second region so as to enhance the heat-dissipation efficiency of the substrate and the integrated circuit chip.

18. The integrated circuit package structure of claim 11, wherein the substrate is electrically connected to a multi-layer circuit board via a plurality of pins.

19. The integrated circuit package structure of claim 18, wherein the multi-player circuit board comprises an isoelectric conducting layer and a plurality of through holes, and the pins are electrically connected to the isoelectric conducting layer via the through holes, and the heat generated by the integrated circuit chip is dissipated via the isoelectric conducting layer.

20. The integrated circuit package structure of claim 19, wherein the isoelectric conducting layer is a power layer or a ground layer.